AMSL3: Optical Receiver Design Documentation

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Additional Key Words and Phrases: Analog Circuit, Optical Receiver

1 INTRODUCTION

BitLight LTd is looking forward to an advanced new optical communication receiver design, which is suitable for the optical fibre communication and visible light communication as well. As a trainee engineer, we are allocated with the tasks of producing an optical receiver desgin in order to achieve the optical data transmission objective. And we are required to satisfy all the conditions that company has given with the smallest cost and the most optimal effect (gain). In this documentation, we have provided a detailed design information about this receiver so that you can check the design, debugging and testing results easily. We also provide the layout and 3D representation of the PCB board, as well as the PCB design diagram. We ensure that it satisfies most of the specifications that has been given although one rule is slightly violated according to our simulations.

2 DESIGN DETAILS

2.1 Trans-impedence Amplifier(TIA)

The input of the entire system is light, which is equivalent to a current signal. We want to achieve voltage rather than current as the output of the optical receiver. Therefore, we need to convert current to voltage in the first stage, which is realized by trans-impedence amplifier(**TIA**). In the simulation, we use a capacitor C_{pd} in parallel with an independent ideal current source to replace the photodiode, which is shown in Figure 1. We have another capacitance C_1 in parallel with a resistance R_1 at the inverting input and output terminal of the op-amp. The total capacitance C_T on the inverting terminal of the op-amp, which is calculated by: $C_T = C_{pd} + C_{in}$. C_{pd} is equal to 2pF, C_{in} is equal to 10pF, therefore C_T is equal to 12pF.

From the V-I characteristic transfer function we know that TIA is a low pass filter,and its -3dB bandwidth(f_{-3dB}) is given by the following formula: $f_{-3dB} = \sqrt{gbw/2\pi C_T R_1}$. Here gbw refers to **Gain Bandwidth Product**, which is the bandwidth of the op-amp at unity gain. The bandwidth should between 5MHz to 8MHz. Since there are many other low-pass filters after the TIA module, they may cause a faster drop to -3dB, so we set the cutoff frequency to approximately but smaller than 8MHz. We choose LM6171 as our main choice of op-map. For LM6171, gbw is equal to 100 (MHz) given ± 15V voltage apply [1]. Therefore, we can calculate R_1, which is 21kΩ. A precise cut-off frequency under this circumstance is 7.947MHz. C_1 is a feedback capacitor which is placed to create a pole in the noise gain function. The optimal C_1 is calculated by: $C_1 = \sqrt{C_T/2\pi R_1 gbw}$, which is 0.95pF in this case. Besides, the gain at this stage is calculated by : $G_1 = |V_{out}/I_{PD}| = |R_1||1 + jwR_1C_1|$, which is approximately equal to 2.08 * 10^4.

2.2 DC Blocker 1

One DC blocker(HPF1) is followed by module TIA, which is a high pass filter to remove any non-data carrying DC from the subsequent stages of the receiver. This module is made up of a capacitor C_2 and a resistance R_2. It is required that the order of the filter should not be less than 1, and the cut-off frequency f_c should not be greater than 2kHz. Assume

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that the cut-off frequency is 900Hz, according the -3dB point. Considering that the next stage is the Sallen key 4th order filter module that may cause loading effects. If R_2 is too large, the gain will be less than expected. Therefore, R_2 should be small enough, which is assumed to be 30 Ω and results in C_2 to be 6 μF. The theoretical cut-off frequency is equal to 884.194Hz. The gain is approximately small for a low frequency. The exact gain for HPF1 is: $G_{HPF1} = R_2/|1/jwC_2 + R_2|$, which is approximately equal to 0.999(1) since the signal frequency is much larger than cut-off frequency.

2.3 Sallen Key Active Filter

A single Sallen key filter consists of four resistors and two capacitors with one non-inverting operational amplifier. This module is used for increasing the signal strength and giving compensation for channel path loss. The specific feature of a Sallen Key filter is that it has a large input impedence but low output impedence with good stability. To meet the design specification, we should desgin a 4-th order low pass filter, a cascade of two Sallen Key active filtered are followed by the first DC blocker, with each 2-th order Sallen key filter. A higher order is also accepted and practical but this may generate potential issues such as unstability (fluctuations) and strong damping effects on the side of filter's ouput. We need to consider cut-off frequency, as well as quality factor Q and damping factor. To ensure the stability of the whole system, we look through the given materials[1]. We find that for a 4th order butterworth filter, the first stage should have a Q factor value of 0.5412 and the second stage should have a Q factor value of 1.3065[1] to reach the optimal frequency response. However, we have two same Sallen Key filter instead with each Q being equal to 1.3065. The reason is that a higher Q leads to a better stability and less damping.

The Q is calculated by: $Q = \sqrt{R_3R_4C_3C_4}/(R_3C_3 + R_4C_3 + R_3C_4(1-K))$, where K(also Gain) is calculated by: $K = G = (R_5 + R_6)/R_5$. So for the first Sallen Key filter, suppose $R_3 = mR_4$ and $C_4 = nC_3$, then $Q = \sqrt{mn}/(m + 1 + mn(1-K))$. To simplify the calculation, we set the same value for both C_3 and C_4, which is 1.0pF here. n = 1 therefore. To make Q equal to 1.3065, according to the eqaution, m is approximately 1.7. In the simulation, we set the R_4 to 5kΩ, which made R_3 to 8.5kΩ. The gain is set to 4 to meet the requirement of voltage gain less than 4V/V, where each filter has a gain of 2V/V. So R_5 is equal to R_6, which is 1kΩ. For the second stage Sallen Key filter, the calculation process is the same as the first stage. R8 is equal to 5kΩ, which made R_8 to 8.5kΩ. R_9 is equal to R_{10}, which is 1kΩ. Both C_5 and C_6 are equal to 1.0pF here. The effect of different values with same ratios for Sallen Key filter is discussed in part 3.6, also with the discussion of cut-off frequency of Sallen Key filter. The desired cut-off frequency is approximately 7.03MHz in simulation.

2.4 Low-pass Filter and Post Amplifier

After the Sallen Key active filter, we add one low-pass filter with one capacitor parallel with one resistance. This LPF is used for limiting the bandwith of transmission and attenuate signals and noise over and above the desired frequency to improve the signal to noise ratio (SNR). Cut-off frequency is calculated by: $f_{LPF} = 1/(2\pi * C_7R_{11})$. This value should be large enough since we want a overall high cut-off frequency but no more than 8Mhz. The desired frequency for this LPF is equal to 8Mhz. In the simulation we set R_{11} to 30Ω and C_7 to 0.7nF, which results in a cut-off frequency of 7.58MHz. We choose a small R_{11} since we've considered the loading effect that will happen at the input of the post amplifier.

Post amplifer is designed after the LPF block, which can provide a higher gain than Sallen Key filter blocks, strengthen the signal to compensate for the channel path loss. We can use cascade inverting amplifiers to realize $G = G_1 * G_2 * G_3 ... * G_n$ or only use single stage amplifier. In real design, we adopt only one inverting op-amp with (+) port connected to the ground and two resistances connected to the (-) port. Total gain G_{IV} for the system should be $V_{out}/I_{DP} = 1V/2 * 10^{-6} = 5 * 10^5$. After the last few modules, the total gain should be: $G = 2.08 * 10^4 * 1 * 4 = 8.32 * 10^4$. We consider the loading effect problem as we've discussed before. R_{12} is set to 10kΩ in simulation. It's reasonable since

it's much larger than R_{11} and the it can be easily found both in lab and in factory. The gain of the post amplifier should be 6.01 to match the total gain of $5 * 10^5$. The theoretical value for R_{13} is equal to 60.1kΩ and we tuned it to 61.1kΩ to let the output match 1V-V peak to peak. The value of R_{14} is 36Ω since open loop resistance of op-amp is 14Ω and we need a output resistance of 50Ω. (Output resistance is calculated by: $R_{out} = R_{14} + R_{13}//R_0$ where output resistance of op-amp R_0 is 14Ω. $R_0 << R_{13}$ so $R_{13}//R_0 \approx R_0 = 14\Omega$, so $R_{14} \approx 36\Omega$

2.5 DC Blocker 2

After the post amplifer, we need to add one DC blocker. The reason is that almost each op-amp, including LM6171 has a dc bias. This violates the rule that the output should not contain DC bias. The cut-off frequency is set to 800Hz. In ltspice simulation, the value of C_8 is equal to 50nF and R_{15} is equal to 4kΩ. The result and discussion of the final DC-offset is shown in part3.1. The gain is approximately 1.

2.6 Overall Schematic Diagram and design summary

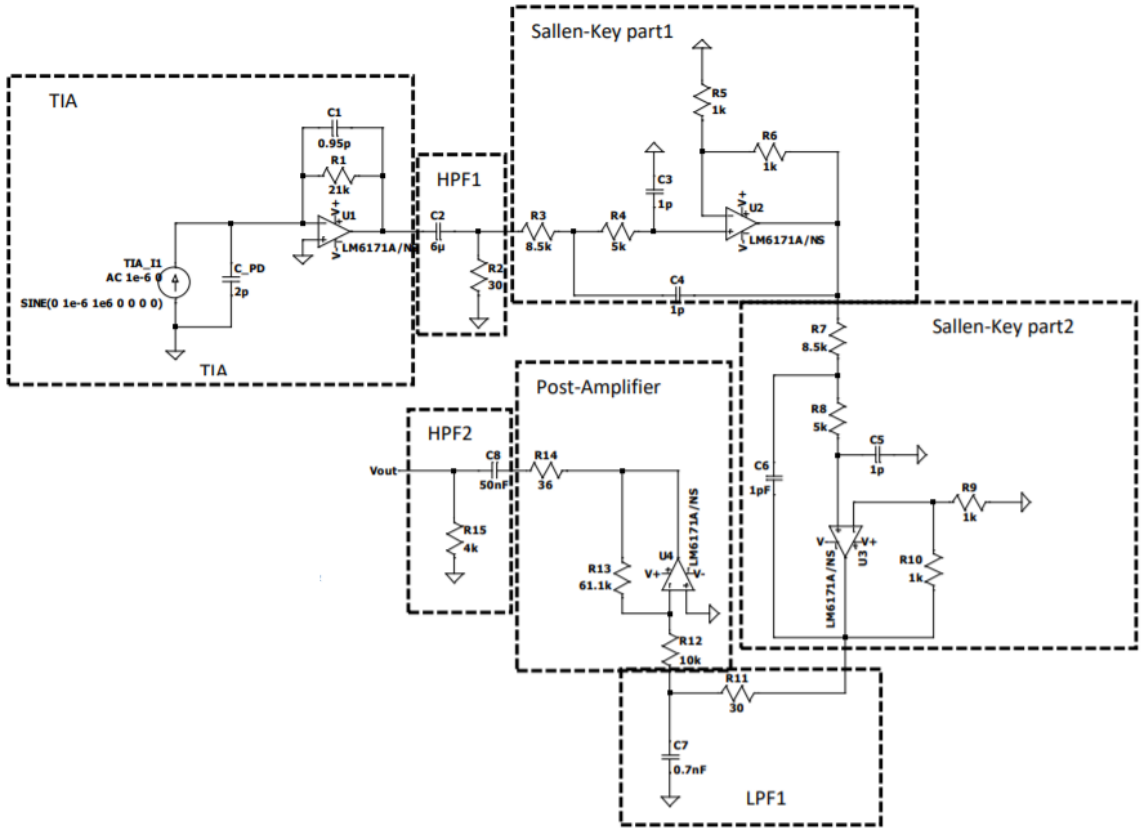

Fig. 1. schematic diagram

This section shows a picture of the schematic diagram, as well a summarized design details in a table.

Table 1 Component values' summary in a table.

Component	Value	Component	Value	Component	Value	Component	Value
C_{PD}	2pF	R_4	5kΩ	R_8	5kΩ	C_7	0.7nF
C_1	0.95pF	R_5	1kΩ	R_9	1kΩ	R_{12}	10kΩ
R_1	21kΩ	R_6	1kΩ	R_{10}	1kΩ	R_{13}	61.1kΩ
C_2	6 μF	C_3	1pF	C_5	1pF	R_{14}	36Ω
R_2	30 Ω	C_4	1pF	C_6	1pF	R_{15}	4kΩ
R_3	8.5kΩ	R_7	8.5kΩ	R_{11}	30Ω	C_8	50nF

3 EXPERIMENTS

3.1 Final design testing

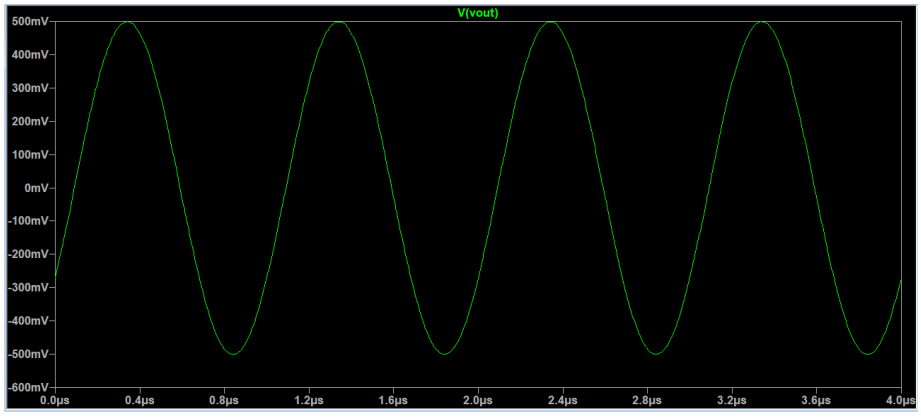

Fig. 2. output waveform from 0μs to 4μs

We should verify that the desined circuit must show a correct behaviour in time domain. The software for verification is based on *ltspice*, where we put our schematic diagram inside and do simulations on. In the independent current source settings, we set the PD signal to *SINE* function. We set the **Amplitude** option to 1e-6 A, **frequency** to 1e6 Hz, **AC amplitude** to 1e-6 while other options are filled or initialized with 0. In order to perform time domain simulation, we use the **Transient Analysis** and simulate for 4μs. (begin time: 0μs, stop time: 4μs)

The results show that we get an amplified version of PD current from the design. The initialized PD current is 2e-6 A(peak to peak) while the output voltage is approximately 1.000V (peak to peak). The V-I gain is approximately 5 * 10^5. So it also satisfies the condition of a proper gain of the optical receiver.

In order to record the peak to peak value of the output waveform accurately, in real tests, we move two cursors onto the upper peak and lower peak of the sine wave. The maximum of the sine wave is 499.02 mV and minimum of the sine wave is -500.63 mV. So peak to peak is 999.65mV. Absolute error is -0.35mV and relative error is 0.035%. The expected value should be 1000 mV here. However, there's a small error. The potential reason is that although Sallen key filter has the correct amplification here in simulation, but our circuit exists loading effect at the end of first DC blocker and at the end of the first low pass filter. In order to compensate for it, I have designed a post-amplifier with a higher gain

than the theoretical one but can not reach a more accurate value since we require the values of components to match industry based values as expected. (This piece of information is also mentioned in designed part)

We can find that although we set the DC blocker after the post amplifier, it does not ensure the absolute maximum and minimum value are equal to each other. The DC offset is equal to (499.02 - 500.63)/2 = -0.805mV. It's small enough but can not be ignored. The reason that the offset is still not equal to zero even if we add the DC blocker is that there exists both dc and ac voltage offset for op-amp, And the ac part is not stable and does not perform as a sine wave though it is small enough. The image still shows the sine wave because it is really small (smaller than 0.5mV when comparing to 500mV). But we should not neglect the effect and should compare the results with using different op-amps and different values of capacitors of the DC blocker to verify this reason further.

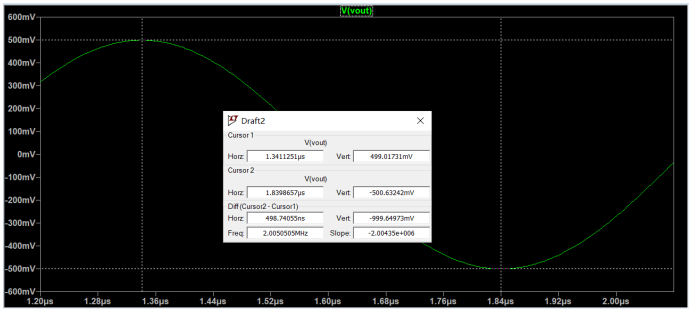

Fig. 3. peak to peak

3.2 Design Characterisation - Frequency response

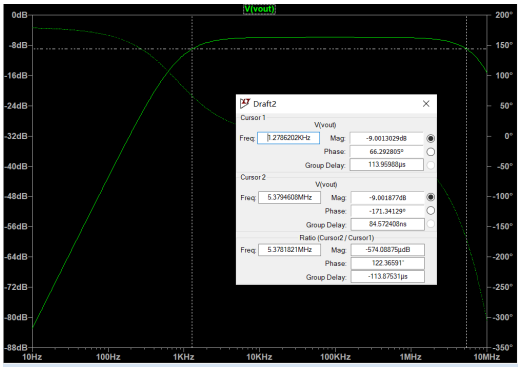

Fig. 4. Frequency response of the system

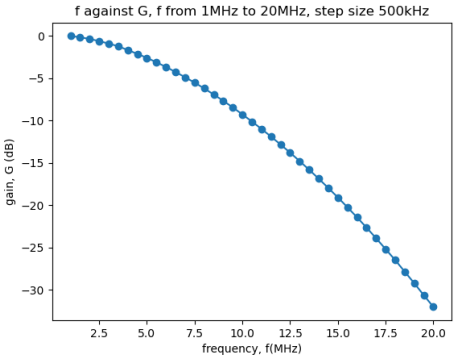

Fig. 5. f against G, f from 1MHz to 20MHz

Besides tests in time domain, it's also important to test frequency response of the circuit where we change the time domain into frequency domain. In LTSpice, we set the PD signal, which is described as a current source, to 'SINE' function but with the same configuration set up as in the final design testing part. In the simulation set up, instead of choosing transient analysis, we transfer to AC analysis with 101 numbers of points each decade from 10Hz to 10MHz, which is shown in figure 4.

The results show that we have designed a perfect band pass filter. The bandwidth is equal to 5.379 MHz - 1.2 kHz = 5.378MHz. It is the expected bandwidth from the design calculation. The Bode plot show that when signal frequency is less than 1.28 kHz, the slope is positive and has a less than -3dB gain. When signal frequency is larger than 5.378 MHz, the slope is negative and has a less than -3dB gain. The slope in the pass band is flat and smooth with no damping effect.

Besides, in order to record the gain more accurately, instead of reading the value in the bode plot of output voltage, we go back to time domain and set the base frequency at 1.0MHz. The aim is to see how the gain varies from a lower frequency to a higher frequency. The maximum frequency step is 0.5MHz in this case. Usually if we want to see the -3dB point, which refers to the cut-off frequency point, we must set a smaller frequency step to realize it. However we set to the maximum step directly. From the table1, we can easily find the frequency which is near to -3dB point, also when frequency is small, decrease of gain is also small enough. When value of signal frequency is ascending, the decrease of gain increases, which means the absolute value of 1st derivative of the stop band slope increases. We plot a frequency response curve of the table1 to confirm this and compare with the frequency response simulation results which is shown in figure 4. The coresponding value in the table can be found in the frequency response achieved from ltspice. The curve shown in figure 5 is part of that frequency response curve in ltpsice.

Table 2 Frequency response and gain under different frequencies between 1 MHz and 20 MHz with a step of 0.5MHz.

Freq, f(MHz)	V_{out} (V)	$V_{out}/V_{out(1e6)}$	G	Freq, f(MHz)	V_{out} (V)	$V_{out}/V_{out(1e6)}$	G
1.0	0.9996	1.0000	0.0000	10.5	0.3118	0.3119	-10.1190
1.5	0.9826	0.9830	-0.1490	11.0	0.2820	0.2821	-10.9915
2.0	0.9600	0.9604	-0.3511	11.5	0.2540	0.2541	-11.8999
2.5	0.9326	0.9329	-0.6032	12.0	0.2280	0.2281	-12.8378
3.0	0.9011	0.9015	-0.9008	12.5	0.2041	0.2042	-13.7997
3.5	0.8695	0.8699	-1.2110	13.0	0.1819	0.1820	-14.7999
4.0	0.8246	0.8248	-1.6717	13.5	0.1616	0.1617	-15.8277
4.5	0.7838	0.7841	-2.1124	14.0	0.1431	0.1432	-16.8837
5.0	0.7419	0.7422	-2.5896	14.5	0.1261	0.01262	-17.9822
5.5	0.6988	0.6991	-3.1095	15.0	0.1110	0.1110	-19.0901
6.0	0.6556	0.6559	-3.6637	15.5	0.0971	0.0971	-20.2521
6.5	0.6122	0.6124	-4.2587	16.0	0.0847	0.0847	-21.4389
7.0	0.5700	0.5702	-4.8790	16.5	0.0736	0.0736	-22.6590
7.5	0.5296	0.5298	-5.5143	17.0	0.0637	0.0637	-23.9137
8.0	0.4894	0.4896	-6.2032	17.5	0.0549	0.0549	-25.2051
8.5	0.4506	0.4508	-6.9207	18.0	0.0473	0.0473	-26.4993
9.0	0.4134	0.4136	-7.6691	18.5	0.0404	0.0404	-27.8689
9.5	0.3778	0.3780	-8.4513	19.0	0.0345	0.0345	-29.2401
10.0	0.3436	0.3437	-9.2755	19.5	0.0293	0.0293	-30.6592
/	/	/	/	20.0	0.0250	0.0250	-32.0377

3.3 Design Characterisation - Step response

In this part, we discuss the stability of our designed system and measure the theoretical bandwidth, as well as record the percentage overshoot in the step response of our design. In ltspice simulation, current source is set to *Pulse function*,

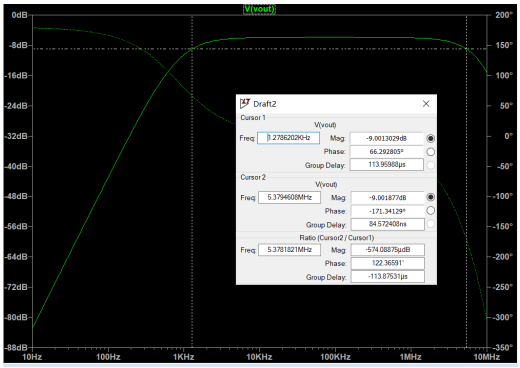

Fig. 6. Frequency response of the system

with I2 equal to $1 * 10^{-6}$A, Ton and Tperiod equal to $4 * 10^{-6}$ and AC Amplitude equal to $1 * 10^{-6}$. Other parameters are equal to zero correspondingly. In transient analysis settings, starting time is 0 μs and the simualtion stops at 4 μs.

We know that the rise is the time taken for the pulse to rise from 10% to 90% of its steady state value. Figure 5 shows the result of step response of our desined system, the the maximum value is 505.8912mV at approximately 240ns. So the 10% and 90% of the maximum value are equal to 50.589mV and 455.302mV respectively. We use two cursors to find these two points when the ouput value is ascending. From the image we can find two approximated times, but they are not accurate enough. Zooming the output wave, more accurate start time and end time are 60.24 ns and 124.15ns. Therefore, rising time t_r becomes 124.15ns - 60.24ns = 63.91ns. Since step response will make the current source value stable, which will become $1 * 10^{-6}$ A, the output value will also be stable and become 500mV. ($1 * 10^{-6}$ sine wave lead to a 1V-V ouput which means $1 * 10^{-6}$ DC wave will lead to 500mV DC voltage.) The percentage overshoot equation is given by: ps = ($V_{maximum}$ - V_{stable}) / V_{stable}. V_{stable} is equal to 500mV where $V_{maximum}$ is equal to 505.8912 mV, which leads percentage overshoot to: (505.8912 - 500) / 500 * 100% = 1.18% . We are satisfied with this value since it's small. Besides, there's no oscillation as we can see in the figure 5 it's maximally flat. The system is stable.

We're also asked to estimate the theoretical 3dB bandwidth of our optical communication receiver. The approximate expression of this theoretical bandwidth is given by: $B_{theoretical} \approx 0.35 / t_r$, where t_r is 63.91ns and has been calculated before. So $B_{theoretical} \approx$ 5.476 MHz. The results in part3.2 *frequency reponse* told us that experimental bandwidth B is equal to 5.378 MHz. Absolute error is 0.098MHz. Relative error is 0.098 / 5.476 = 1.79%. The result shows that the relative error is small. The estimated theoretical bandwidth is larger than the measured bandwidth from frequency response. One part of error is caused by the estimation of ln(9)/2$\pi \approx$ 0.349 to 0.35 while other errors may come from the rising time estimation. The expected value should be larger than the current value. Anyway, it's just simulation so a 1.79% relative error is allowed. From the experiments in this part we can also verify that our design is perfect.

3.4 Verification for each module

To indicate that each part has been designed as the specification requires, we show the frequency response after each individual part and the results of total system frequency response has been already shown in part 3.2.

For TIA, the frequency repsonse is without expectation. Even if we move away the following modules, the cut-off frequency is 10.6MHz, which might result from the different value of C_T in simulation. In simulation this value is smaller than the theoretical one. After the module HPF2, measured cut-off frequency is 884Hz and is close to the theoretical

value. The bandwidth for the Sallen Key filter is 6.94 MHz and the bandwidth for the LPF1 is 7.56 MHz. They are also close to the theoretical value.

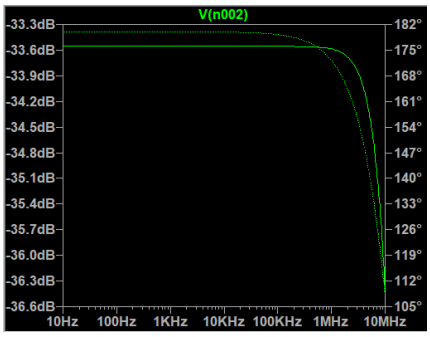

Fig. 7. TIA

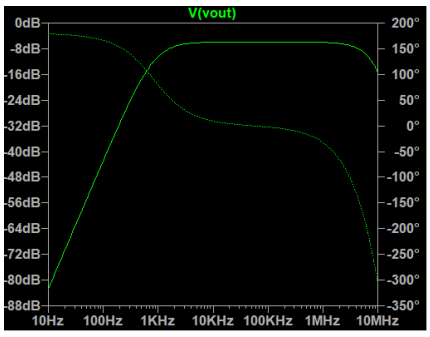

Fig. 8. HPF2

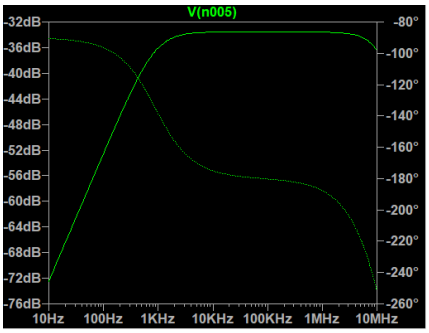

Fig. 9. HPF1

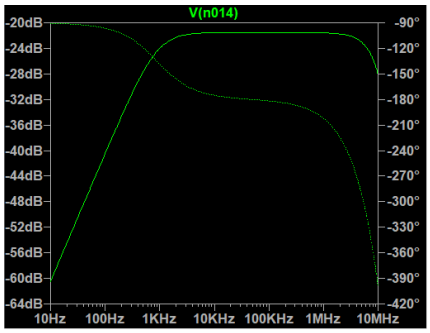

Fig. 10. Sallen Key filter

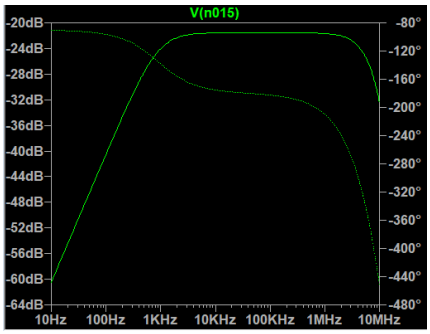

Fig. 11. LPF

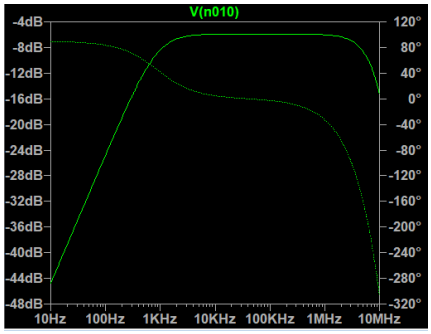

Fig. 12. Post Amplifier

3.5 PCB layout

We design the PCB board in the Target3001! software. Firstly we need to draw schematic diagram the same as the one we've done in *ltpsice*. Several components are being replaced such as the input current source and ground symbol. Input should be only a single photodiode where we choose **BPW32**. Although the information of manufacturer and

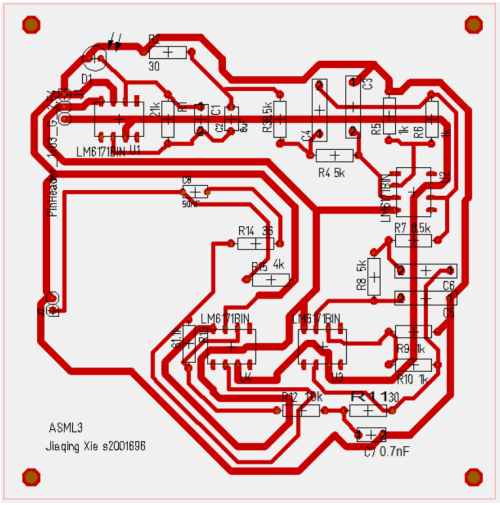

Fig. 13. PCB board

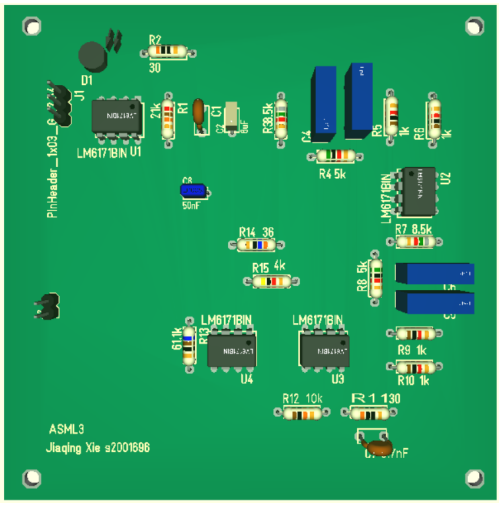

Fig. 14. 3D representation

descriptions are lost, the pitch is 2.54 mm which is smaller than 6mm and is suitable for a lab PCB routing. We use two pin headers, one 2-pin and another one 3-pin to avoid linking components to the ground directly, as well as the situation for two voltage supplies. We choose the appropriate material which is made of carbon where pitch is 7.62 mm. Considering that capacitors are made of different materials according their values. A 10 μF capacitor can not be the same size as a 1 pF capacitor. For a larger capacitor in the first HPF module, we choose **3X5R5, 08**, while we choose **6X3R5, 08** for the capacitors in other modules. Especially, the routing tests will not be passed if we do not change the size from C_3 to C_6, which will give the spacing errors. Under this circumstance, we change the category of capacitor to 4X14R10, 16. For the op-amp, since we have determined to use LM6171 as the main op-amp and we are required the PCB to be through-holed, we choose **LM6171BIN, DIL8**. Layout of the whole PCB board is similar to schematic diagram. More specifically, it starts at top-left of the PCB board, and it goes from top-left to top-right, from top-right to bottom-right, from bottom-right To bottom left. The output and ground should be connected to the 2-pin header port1 and port2 individually. The size of PCB board is 102.87 mm * 103.505 mm.

Pros are apparent while cons are also obvious. We are satisfied with the routing because of its clearness and well-organized layout. The board size is small so that it saves cost of creating a larger PCB board. On the other hand, electrical components are logically placed on the PCB board so that you can easily know the functions of each block on PCB board. The pin header is easy to find so that it's convenient for you to connect the output to oscilloscope in the lab. One of the most significant cons is the blank space in the middle. We can not eliminate this space because when we move these components at the bottom to the middle, the routing algorithm will not succeed. We have tested several situations where $R_{11}, C_7$and R_{12} are placed at the blank place, the routing algorithm runs for 50 - 60 iterations but no solutions are given at 1-side routing. And this experiment has been executed in Altium Designer. Another obvious con is the cost of materials except PCB board. We figure out that there are four kinds of capacitors on the PCB boards with four of them at a very large scale. Besides, the choice of LM6171 costs us £2.5 for each op-amp while each of LM318 costs us £1. We have four op-amps in total, which costs us £6 more.

3.6 Discussions

There are four aspects that we cast light on, which are the choice of op-amps, effect of choosing Q factor and damping factor, loading effect in the circuit and discrepancy of theoretical bandwidth.

LM6171 is expensive, but the unity gain bandwidth is large for LM6171, which is 100MHz. The unity gain bandwith is small for LM618, which is 15MHz. So when it comes to choose the component values for the Sallen Key filter, we need to consider the unstability since the theoratical bandwidth for each Sallen filter is over 20MHz although overall bandwidth is approximately 7MHz in simulation. LM618 might cause such unstability. Also, output open loop resistance is not given for LM318. We also consider different values of quality factor value for each Sallen Key filter. When we choose the optimal Q value of the 4th order Butterworth filter given by the manual, we found that a larger Q made the system stable and no peaking/ringing at the output. However, choosing a large Q will sacrifice for a large bandwidth. If we choose 0.6 for the first SK filter, we figure out that there will be a serious ringing effect at the post amplifer side. So it's the tradeoff between a large bandwidth and Q factor. The damping factor is defined as 1/(2*Q). A large quality factor leads to a small damping factor, making the system stable.

The loading effect is also under consideration in this project. It appears at the output of **HPF1** and **LPF1**. R_3 must be much greater than R_2 while R_{12} must be much greater than R_{11} to avoid loading effect. We cannot ignore the loading effect. Although you can achieve the final system frequency response by neglecting loading effect, you should check whether internal components obey the design rules. One interesting observation from the simulation is that if we set each Sallen Key filter each bandwidth from 5MHz to 8MHz according to the equation, the final frequency reponse bandwidth will be far less than the boundary of 5MHz. For each bandwidth with 8MHz will make the system bandwidth of 1.8MHz to 1.9MHz. The experiments show that if we want to let bandwidth located in the range of 5MHz to 8MHz, each bandwidth should be more than 15MHz. It is reasonable since we need to find 3-dB point. Slope of LPF is no longer -20dB/decade, instead it's -40 dB/decade.

4 CONCLUSIONS AND IMPROVEMENTS

In this documentation, we design each part for our optical receiver, including a trans-impedence amplifier (TIA), two high pass filters, a 4th order band pass filter, a low pass filter and a post amplifer. Each of the design obey the specification rules although the performance of TIA seems to be slightly wrong in the simulation. We've tested each part in the simulation, together with the final design testing in time domain to check if the output peak to peak is 1V-V, the frequency response and the step response. We've designed PCB layout and shown a 3D representation version of PCB board for production. Many improvements can be done to achieve better performance. For example, the bandwidth of the system has no enough space at all. We can tune the SK filter to let the bandwidth higher to accept signal with higher frequencies. Besides, on the side of PCB design, we can minimize the PCB baord size by locating the components more concentrated. Much appreciation for viewing this documentation and enjoy your design.

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